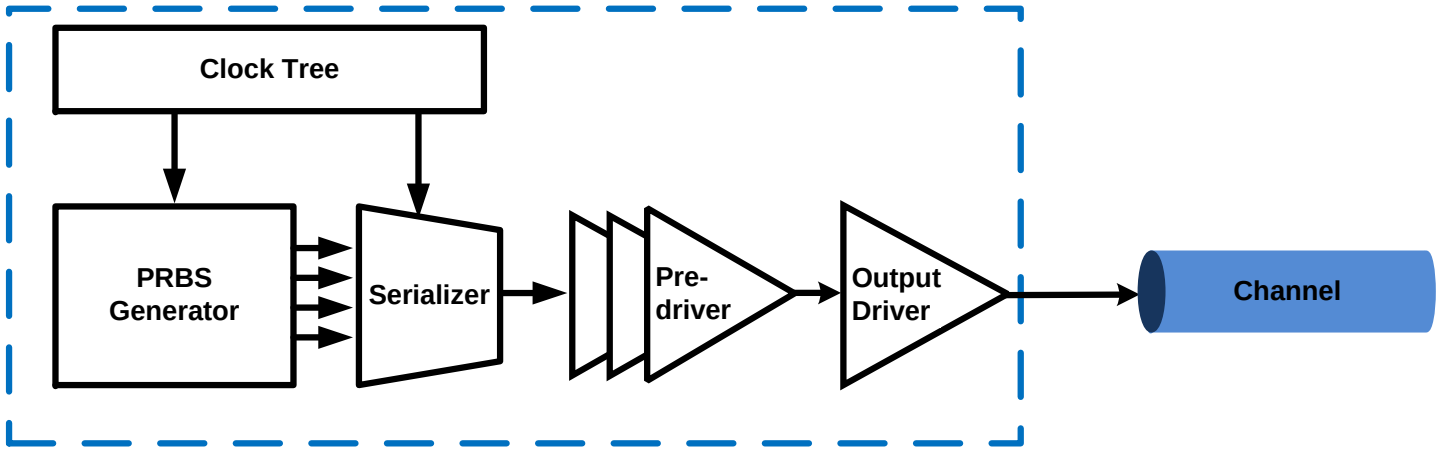
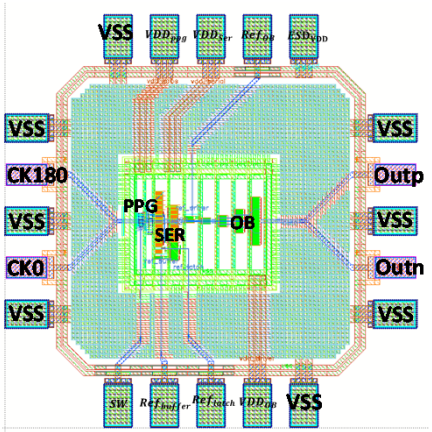
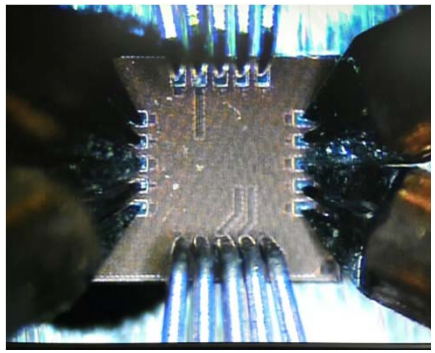
Transmitter in SERDES System

- 10Gb/s transmitter with PRBS pattern generator for BER test

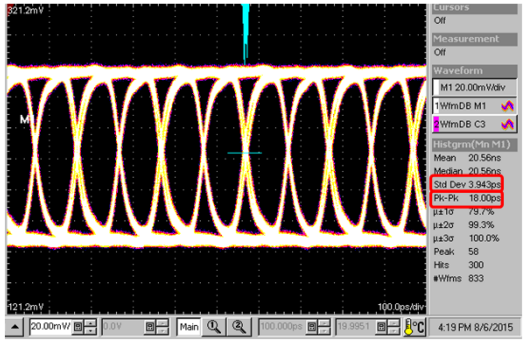




Chip Layout



Chip Photo



10Gb/s eye diagram

Power optimized design of 32:1 transmitter

- **Power-optimized design of transmitter implemented in multi-phase MUX and shift-register**